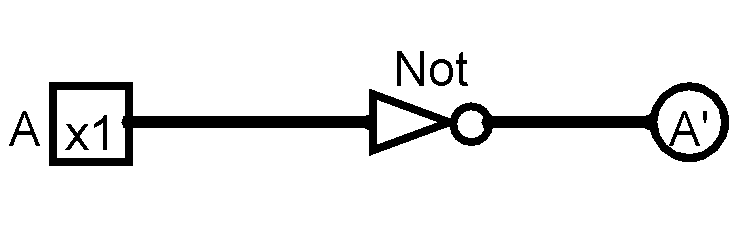
Q1. NOT function

Formulae: A = A’

Truth Table:

|  |  |
| --- | --- |
| A | A’ |
| 1 | 0 |
| 0 | 1 |

Logic Diagram:



Discussion:

Input A is connected to a NOT gate, and the NOT gate is connected to the LED output A’.  
The operation of the circuit is to provide the complement/negation of the input.

The verification is done by the poking tool, if the input A is set to 1 the LED output A’ doesn’t light up but if the input A is set to 0, the LED output A’ shows the red light.

Q2. AND Function:

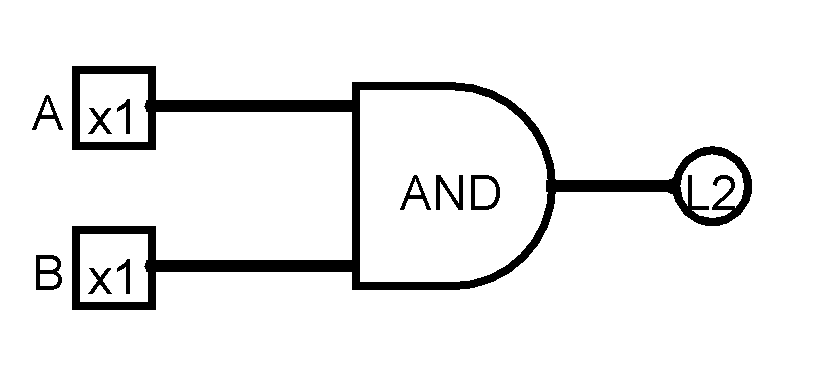
Formulae: L2 = A•B

L2 = A and B , L2 = A & B

Truth Table:

|  |  |  |
| --- | --- | --- |
| A | B | A•B |
| 1 | 1 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 0 | 0 | 0 |

Logic Diagram:



Discussion:

Input A and B is connected to the 2 pin AND Gate, the AND Gate is connected to the LED output L2.

The operation of the circuit is a Boolean “And” operation on two inputs, A and B.

The verification of the function can be seen from the Truth table and by using the poking tool, when Input A and B , both are turned to 1, the LED output L2 lights up to Red, while with every other combination the LED doesn’t light up.

Q3: OR function

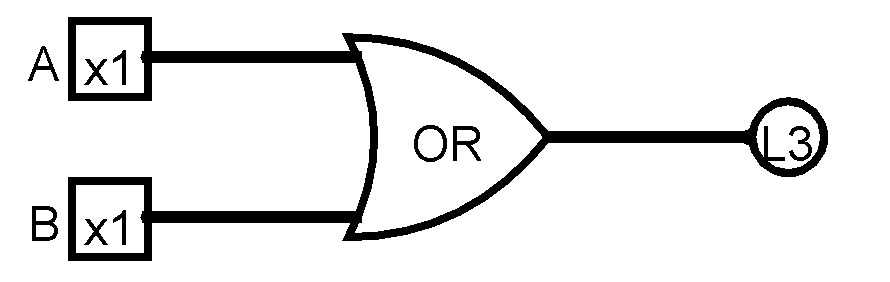
Formulae: L3 = A + B

L3 = A or B, L3= A v B

Truth Table:

|  |  |  |
| --- | --- | --- |
| A | B | A+B |
| 1 | 1 | 1 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 0 | 0 | 0 |

Logic Diagram:



Discussion:

Input A and B is connected to the 2 pin OR Gate, the OR Gate is connected to the LED output L3.

The operation of the circuit is a Boolean “OR” operation on the two inputs, A and B.

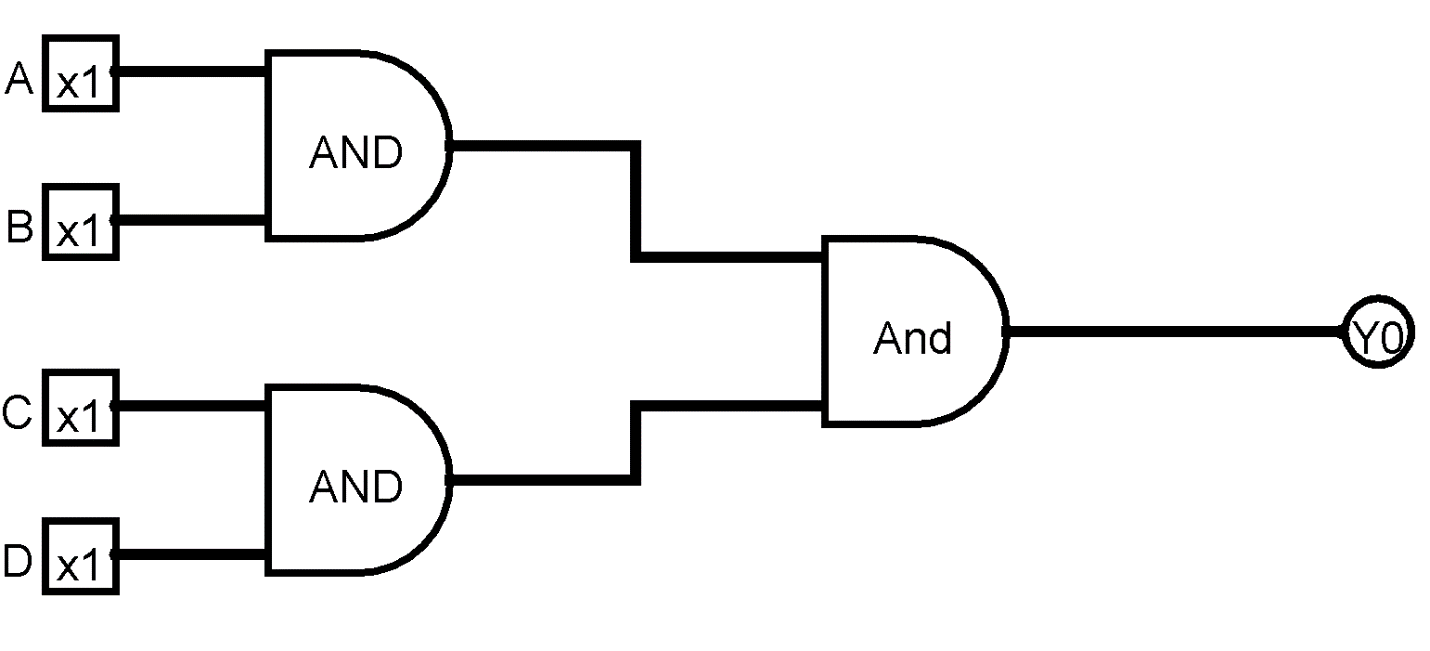
The verification of the function can be seen from the Truth table and by using the poking tool, when Input A and B , both are turned to 0, the LED output L3 doesn’t light up, while with every other combination the LED lights up to red.

Q4: Formulae: **Y0=(A**•**B)** • **(C**•**D).**

Truth table:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| A | B | C | D | **A**•**B** | **C**•**D** | **(A**•**B)** • **(C**•**D).** |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Logic Diagram:



Discussion:

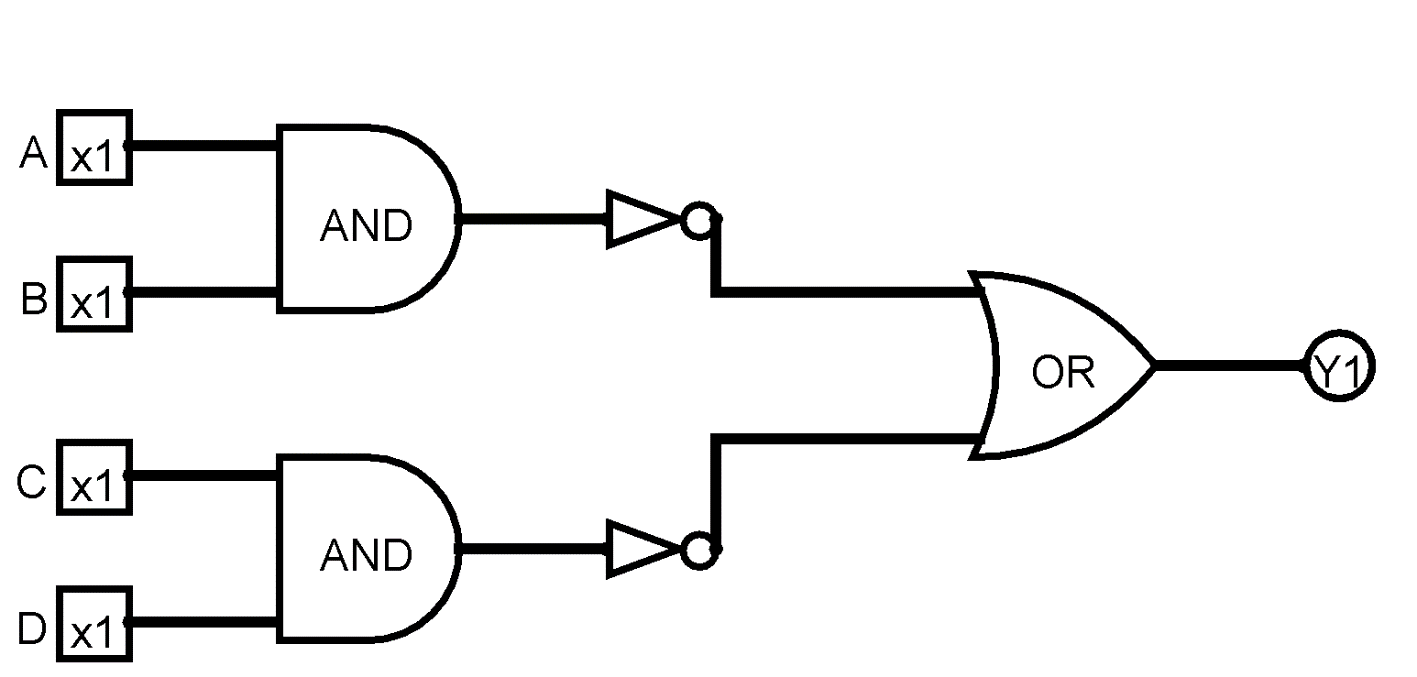
Input A and B is connected to a 2 pin AND gate, Input C and D is connected to another 2 pin AND gate, Both the 2 pin AND gates are connected to another 2 pin AND gate, and the AND gate is connected to the LED output Y0. The operations of the circuit are Boolean “And” operations of input A and B, input C and D, and the results of the all the inputs. The verification of the function can be seen from the Truth table and by using the poking tool, the LED only lights up red when all the inputs, A B C and D are 1.

Q5: Formulae **Y1 = [~(A** • **B)] + [~(C** • **D)]**

Truth table:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| A | B | C | D | **(A** • **B)** | **~(A** • **B)** | **(C** • **D)** | **~(C** • **D)** | **[~(A** • **B)] + [~(C** • **D)]** |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |

Logic Diagram:



Discussion:

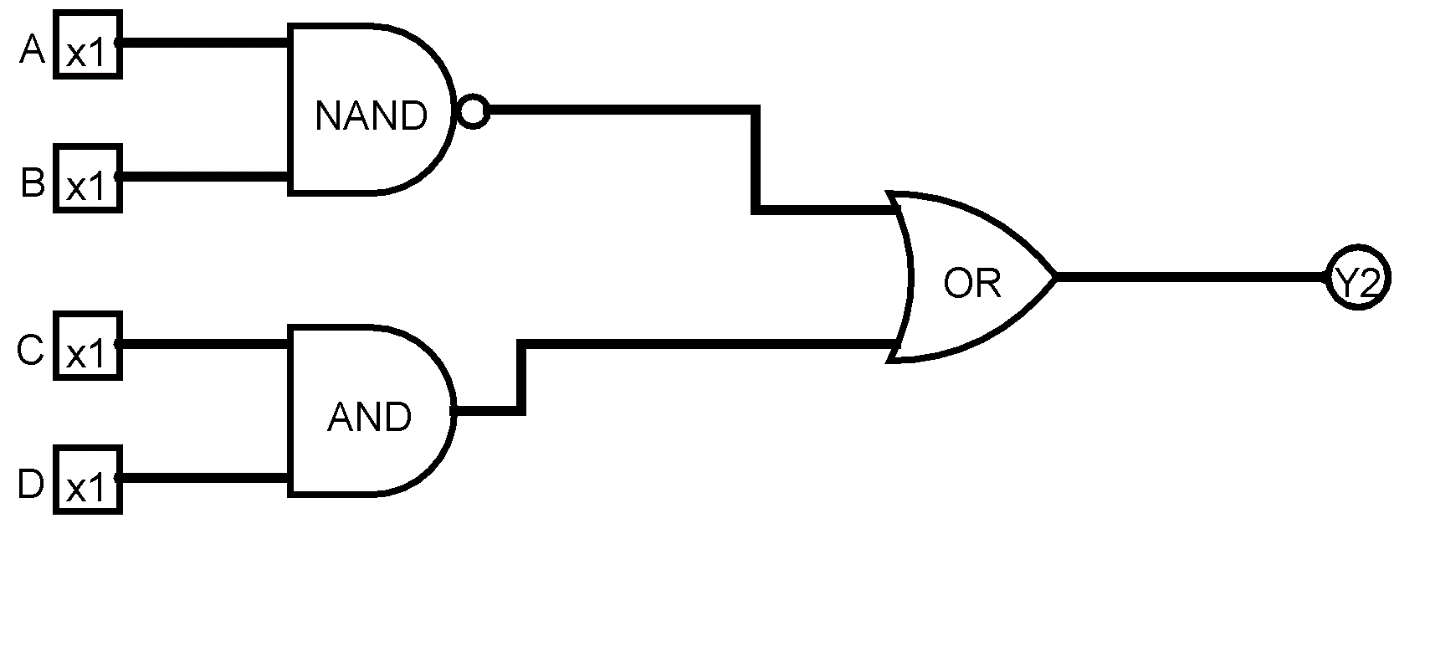
Input A and B is connected to an 2 pin AND gate, Input C and D is connected to another 2 pin AND gate, the AND gates are connected to 1 pin Not gates, and the NOT gates are connected to an 2 pin OR gate, and the OR gate is connected to the LED output Y1. The operations of the circuit are Boolean “And” operations of input A and B, input C and D, Boolean “NOT” operation on the following results of the AND, and Boolean “OR” operation on the results of the NOT . The verification of the function can be seen from the Truth table and by using the poking tool, the LED output Y1 is seen to be turned off when the input A B C and D is 1. While with every other combination of the inputs the LED Y1 lights up to red.

# Q6: Formulae: Y2 = ~(A • B) + C • D

Truth Table:

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| A | B | C | D | **(A** • **B)** | **~(A** • **B)** | **(C** • **D)** | ~(A • B) + C • D |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

Logic Diagram:



Discussion:

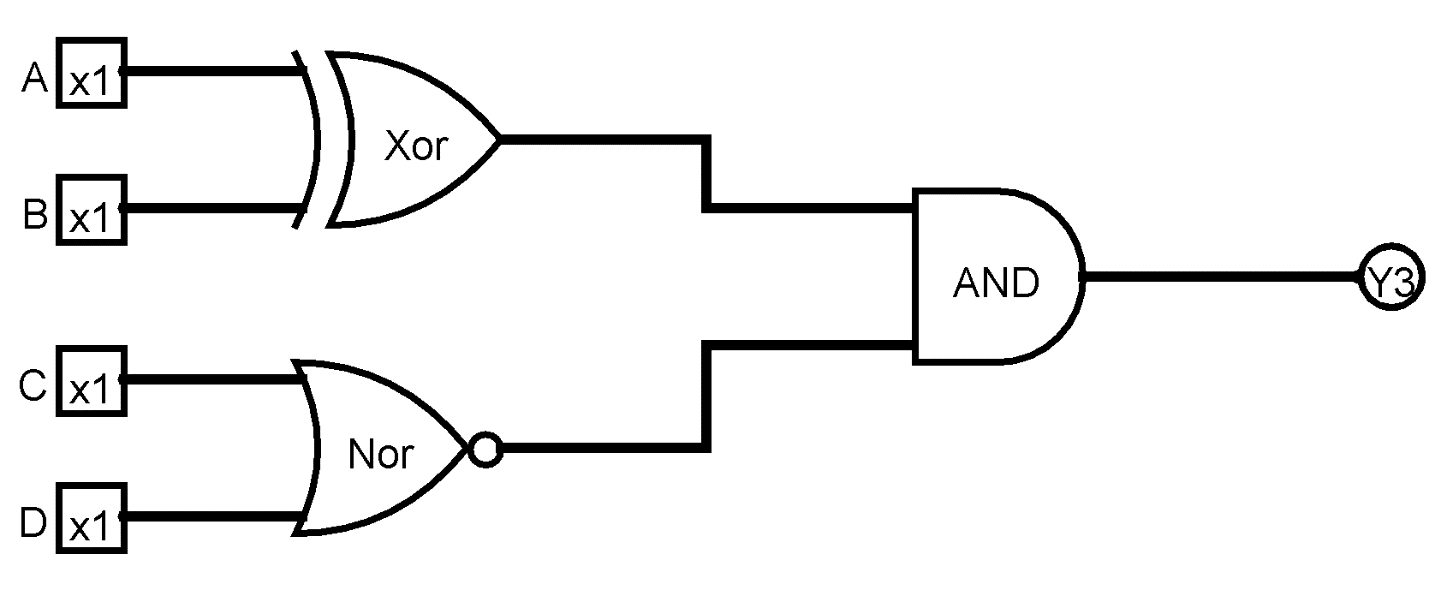
Input A and B is connected to an 2 pin NAND gate, Input C and D is connected to 2 pin AND gate, the NAND gate and the AND gate are connected to 2 pin OR gate, and the OR gate is connected to the LED output Y2. The operations of the circuit are Boolean “And” operations of input A and B along with Boolean “Not” operation making it a NAND gate, Boolean “AND” operation on the input C and D , and Boolean “OR” operation on the results of the NAND and the AND gates . The verification of the function can be seen from the Truth table and by using the poking tool, the LED output Y2 is seen to be turned off when the input A B C and D are, 1 , 1 , 1, 0 respectively, 1 , 1 , 0, 1 respectively, and 1 , 1 , 0, 0 respectively . While with every other combination of the inputs the LED Y2 lights up to red.

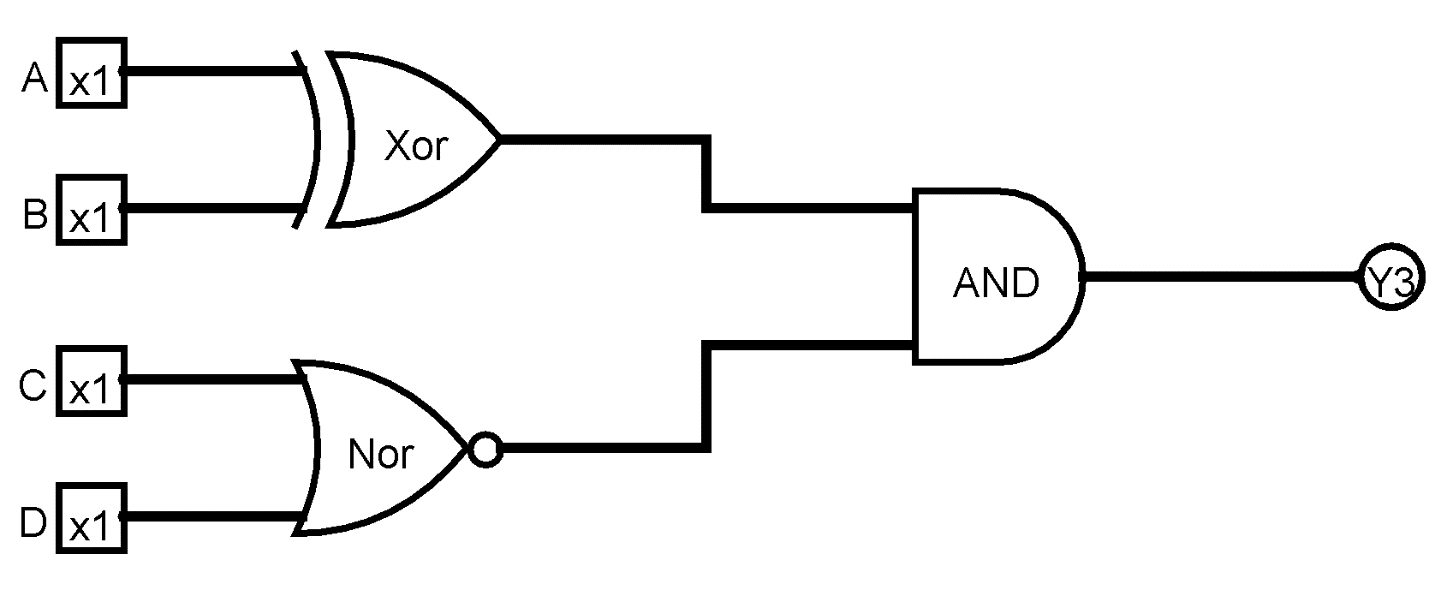
Q7: Formulae: **Y3 = (A** ⊕ **B) • ~(C + D)**

Truth Table:

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| A | B | C | D | **(A** ⊕ **B)** | **(C +** **D)** | **~(C +** **D)** | **(A** ⊕ **B) • ~(C + D)** |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

Logic Diagram:





Discussion:

Input A and B is connected to an 2 pin XOR gate, Input C and D is connected to 2 pin NOR gate, the XOR gate and the NOR gate are connected to 2 pin AND gate, and the AND gate is connected to the LED output Y3. The operations of the circuit are Boolean “Exclusive OR” operations of input A and B , Boolean “NOT” operation along with Boolean “OR” operation on the input C and D making it a NOR operation, and Boolean “AND” operation on the results of the XOR and the NOR gates . The verification of the function can be seen from the Truth table and by using the poking tool, the LED output Y3 is seen to light up red when the input A B C and D are, 1 , 0 , 0, 0 respectively, and 0 , 1 , 0, 0 respectively. While with every other combination of the inputs the LED Y3 does not light up.

Full lab screenshot:

